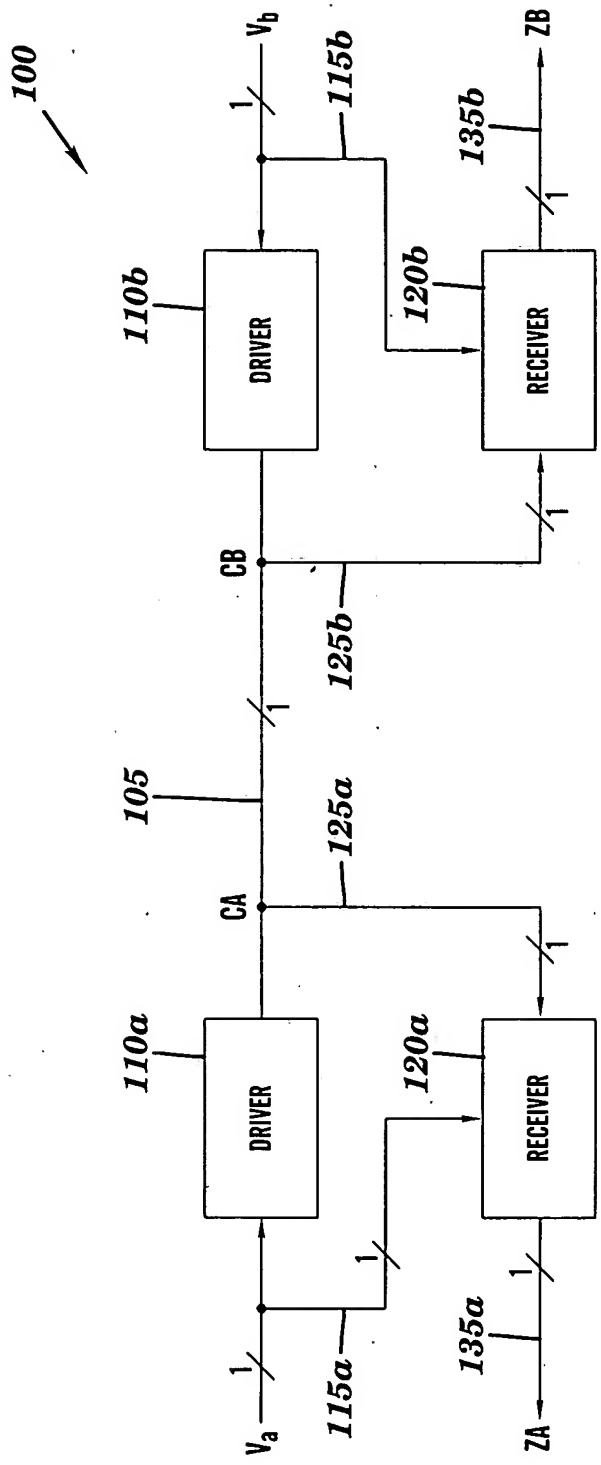
100
105
110a
110b
115a
115b
120a
120b
125a
125b
135a
135b
DRIVER
DRIVER
RECEIVER
RECEIVER
CA
CB
1
1
1
1
1
1
1
1
V_a
V_b
ZA
ZB

FIG. 1

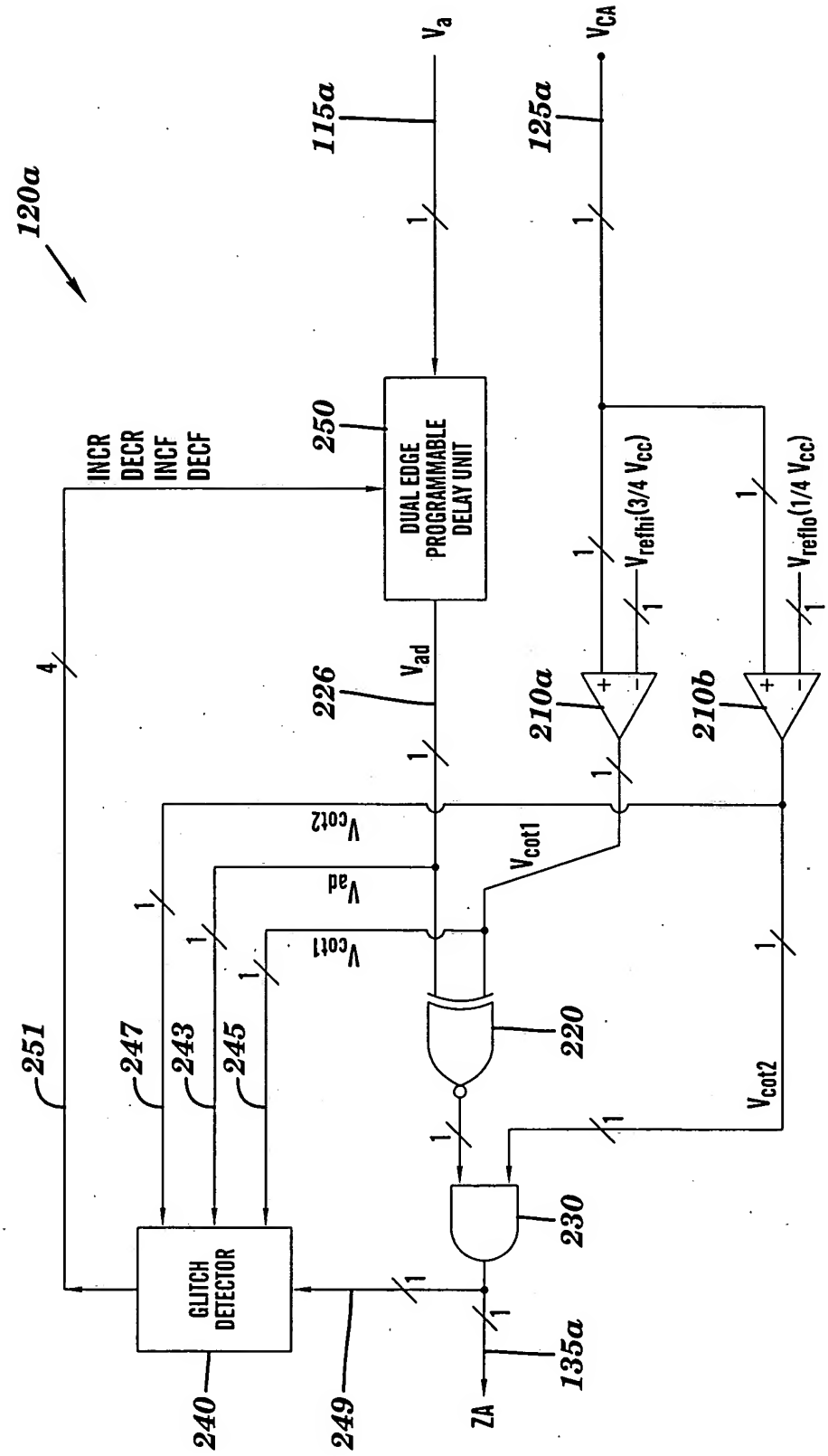
120a
115a
125a
V_a
V_{CA}
250
DUAL EDGE PROGRAMMABLE DELAY UNIT
INCR
DECR
INCF
DECF
4
226
V_{ad}
210a
210b
V_{refhi}(3/4 V_{cc})
V_{reflo}(1/4 V_{cc})
V_{cot2}
V_{ad}
V_{cot1}
220
230
251
247
243
245
GLITCH DETECTOR
240
249
ZA
135a

FIG. 2

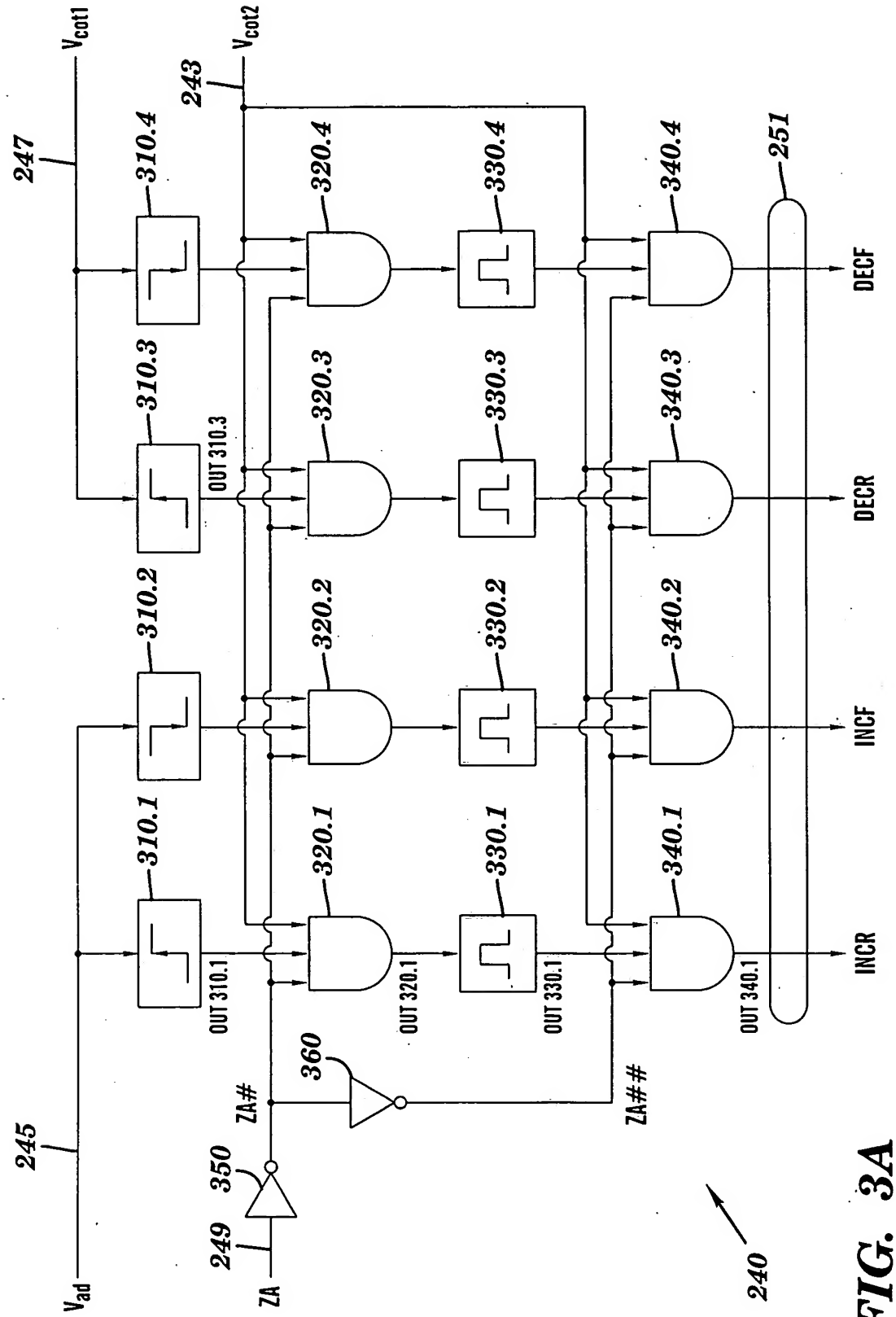
V_{cot1}
V_{cot2}
247
243
245
249
251
310.1
310.2
310.3
310.4
320.1
320.2
320.3
320.4
330.1
330.2
330.3
330.4
340.1
340.2
340.3
340.4
350
360
OUT 310.1
OUT 310.3
OUT 320.1
OUT 330.1
OUT 340.1
ZA
ZA#
ZA##
V_{ad}
INCR
INCF
DECR
DECF
240

FIG. 3A

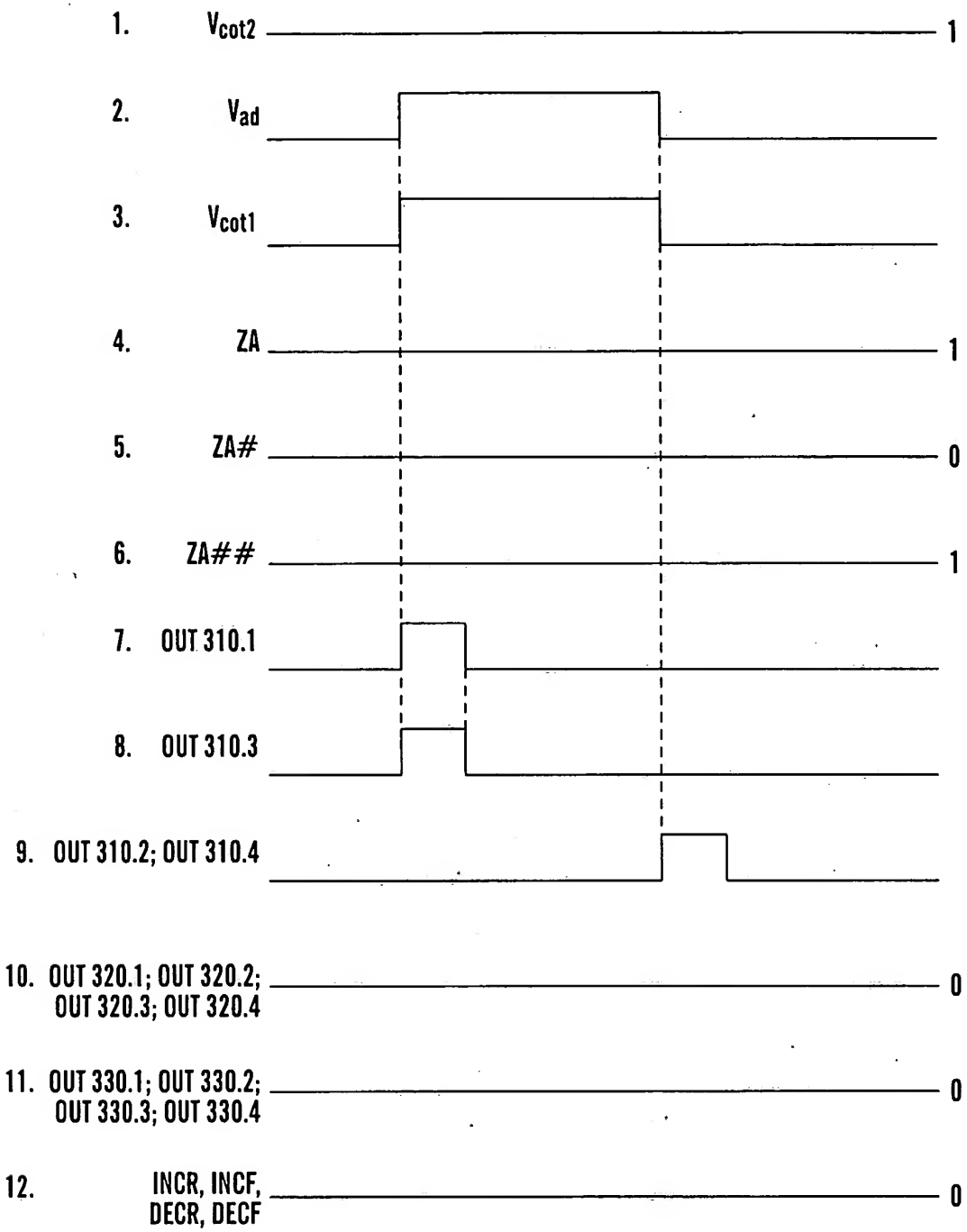
1. Vcot2
1
2. Vad
3. Vcot1
4. ZA
1
5. ZA#
0
6. ZA##
1
7. OUT 310.1
8. OUT 310.3
9. OUT 310.2; OUT 310.4
10. OUT 320.1; OUT 320.2; OUT 320.3; OUT 320.4
0
11. OUT 330.1; OUT 330.2; OUT 330.3; OUT 330.4
0
12. INCR, INCF, DECR, DECF
0

FIG. 3B-1

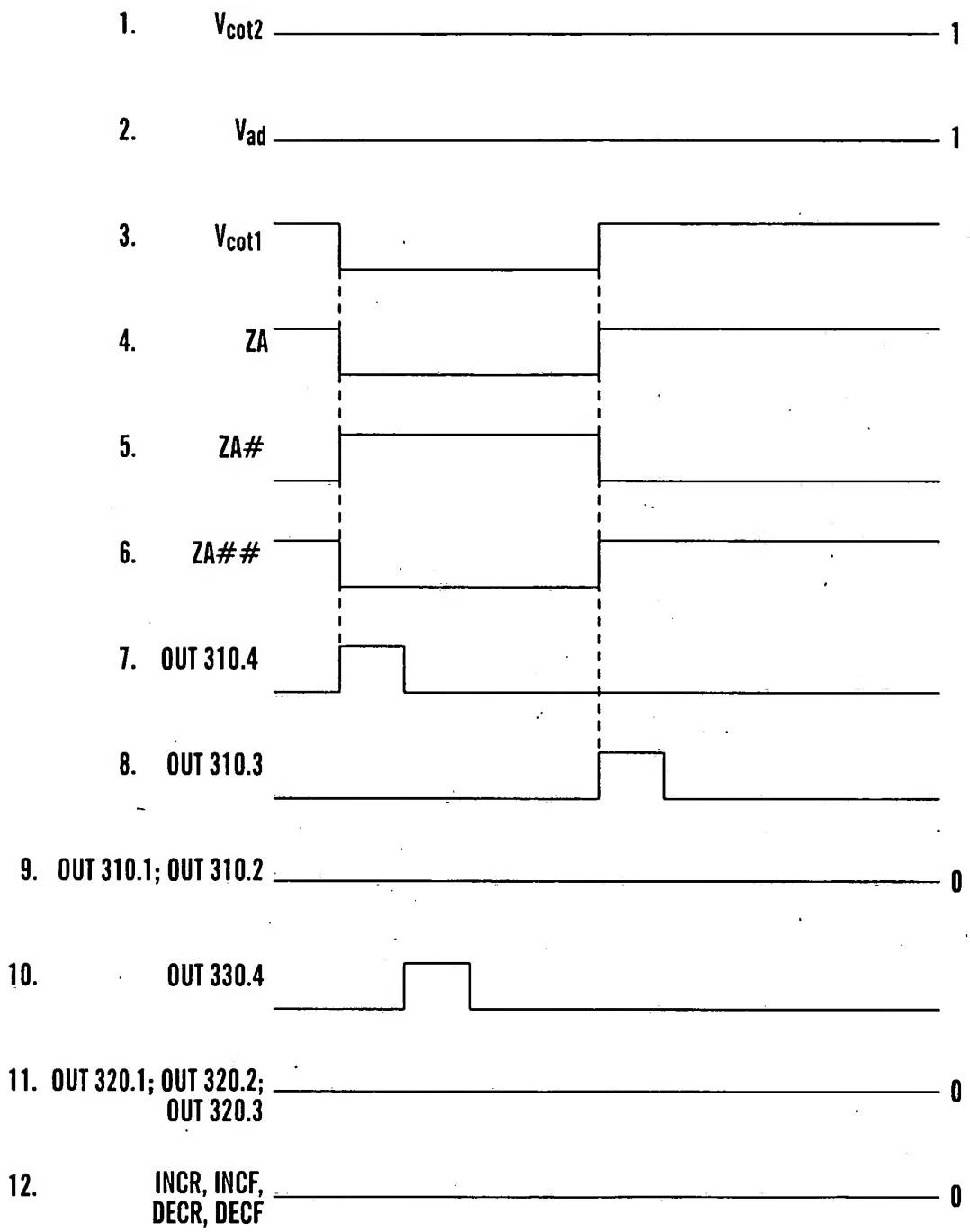
1. V_{cot2}
1
2. V_{ad}
1
3. V_{cot1}
4. ZA
5. ZA#
6. ZA##
7. OUT 310.4
8. OUT 310.3
9. OUT 310.1; OUT 310.2
0
10. OUT 330.4
11. OUT 320.1; OUT 320.2; OUT 320.3
0
12. INCR, INCF, DECR, DECF
0

FIG. 3B-2

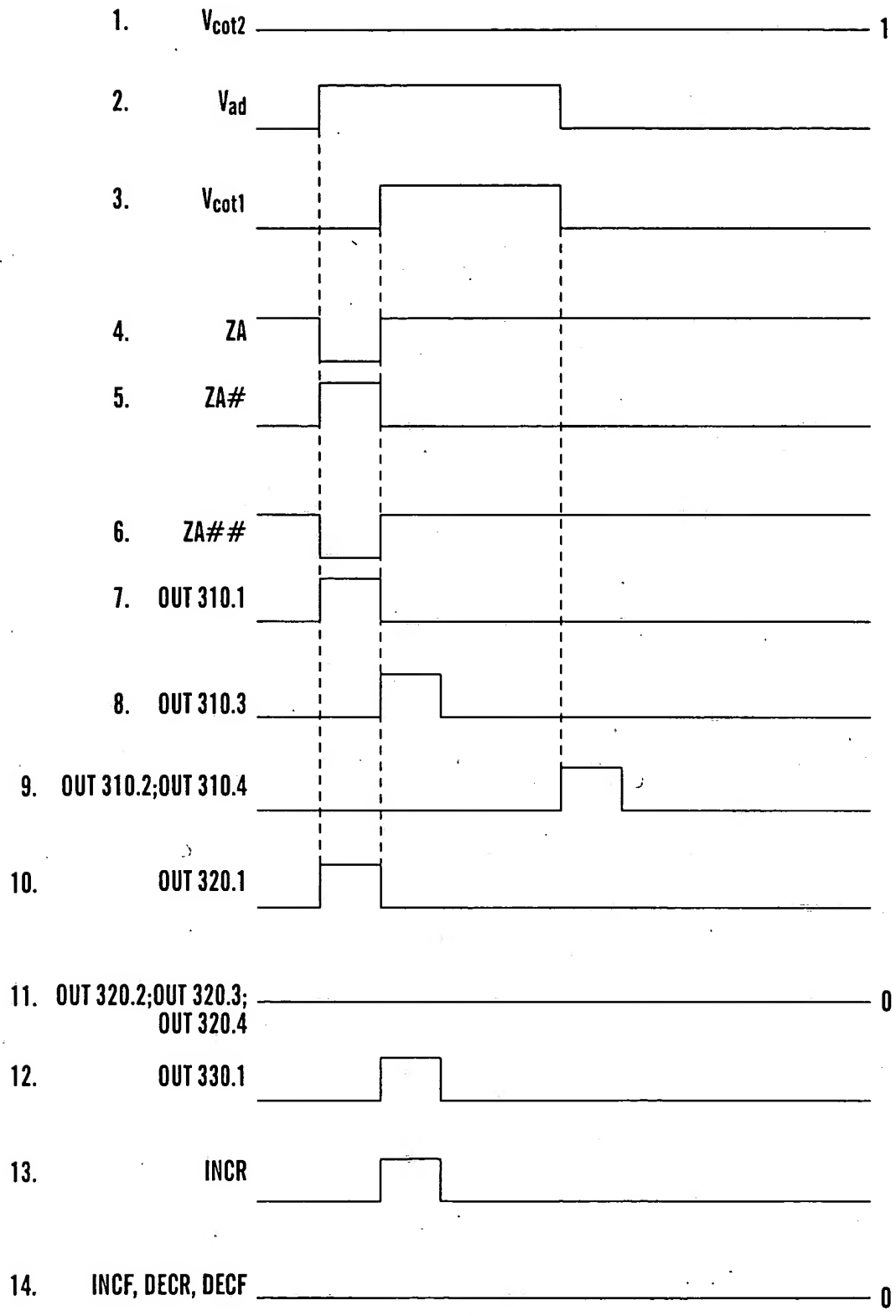
1. Vcot2
1
2. Vad
3. Vcot1
4. ZA
5. ZA#
6. ZA##
7. OUT 310.1
8. OUT 310.3
9. OUT 310.2;OUT 310.4
10. OUT 320.1
11. OUT 320.2;OUT 320.3; OUT 320.4
0
12. OUT 330.1
13. INCR
14. INCF, DECR, DECF
0

FIG. 3B-3

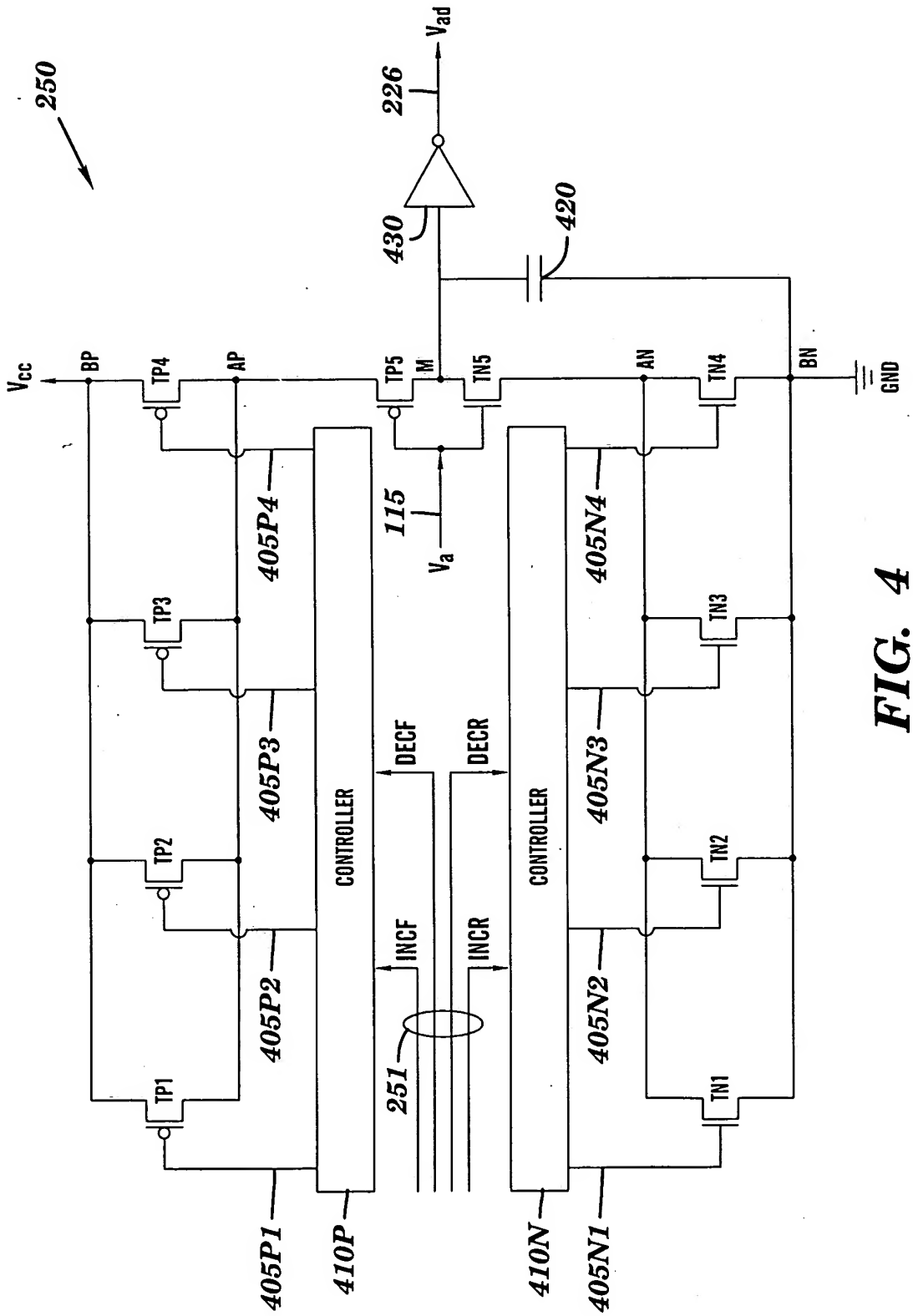
250
226
V_{ad}
430
420
V_{cc}
BP
TP4
AP
TP5
M
TN5
AN
TN4
BN
GND
115
V_a
405P4
405N4
TP3
TN3
405P3
405N3
CONTROLLER
DECF
DECR
CONTROLLER
TP2
TN2
405P2
405N2
INCF
INCR
251
TP1
TN1
405P1
410P
410N
405N1

FIG. 4